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EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/835,021	FELDMAN, ARNOLD R.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-6,17-21,23-25 and 27-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-21,25,31,33-35,37 and 38* is/are allowed.

6)☒ Claim(s) *3-6,23,24,27-30,32,36,39 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

The amendment submitted on Jun 3, 2003 has been reviewed and considered with the following results:

The amended claims overcame the rejections of claims 27-30 under 35 U.S.C. 112 as described in the previous Office Action. Therefore, those rejections have been withdrawn. However, it is believed the amended change to "when the RF signal has an amplitude of zero volts" is misleading and not supported by the original disclosure. Therefore, new rejections of claims 27-30, under 35 U.S.C. 112, are described later under the appropriate section.

Although the amended claims overcame all of the prior art rejections described in the previous Office Action, those previous rejections have now been modified to account for the added limitation (i.e. with respect to the relationship between the gate-source voltages and threshold voltages) now recited within independent claims 3, 6, and 23. For example, the newly added limitation created a new concern about when the transistor biasing actually occurs. This is described in the Rejections under 35 U.S.C. 112 section. Since the previous Office Action's prior art rejections have now been withdrawn, the modified rejections are described later under the appropriate section.

Also, some of the newly added claims created their own problems as described under the 35 U.S.C. 112 section.

Claim Rejections under 35 USC § 112

Claims 27-30 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for having a gate-source voltage approximately equal to the threshold

voltage of a transistor/device at the time when the average of the RF signal is zero, or there is no RF signal, does not reasonably provide enablement for operating near cutoff when "the RF signal has an amplitude of zero volts." The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. As presently understood, it appears the first and second devices of claim 27 will operate near cutoff when the RF signal has zero volts. However, doesn't the cutoff/threshold voltage of the invention actually correspond to the RF signal's zero average (e.g. the level at which the summed voltages of the first and second polarities cancel each other out), and not zero volts?

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-6, 23-24, 32, 36, and 39-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear when the transistors (or devices) "are biased to have gate-to-source voltages approximately equal to their threshold voltages" as now recited within claims 3, 6, 23, 32, 36, and 40. For example, one of ordinary skill in the art realizes a threshold voltage of a transistor corresponds to the switching level controlling when the transistor turns on or off. When an input signal to the control electrode (i.e. gate) of a MOS transistor varies over time, its gate-source voltage also varies. In the case of an NMOS transistor, when the input signal goes above the threshold voltage, the transistor begins to conduct. If the input signal falls below the threshold voltage, the transistor turns off. Therefore, whether the input signal is increasing, or decreasing, the transistor's gate-source voltage will be

approximately equal to the threshold voltage for a period corresponding to when the input signal transitions past the transistor's threshold voltage.

Claim 39 recites the limitation "the seventh device" in line 1 with insufficient antecedent basis for this limitation in the claim. Therefore, it is not clear if it was meant to refer to claim 37's "fifth device", or if sixth and seventh devices were intended to be recited within either claim 37 or 39. [For example, claim 17 clearly recites the first-seventh devices.]

Dependent claims carry over the rejection from claims upon which they depend.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

In so far as being understood, claims 3, 4, 23, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Lincoln, a reference cited in the previous Office Action. Fig. 10 of Lincoln shows a buffer type circuit 1008,1010 receiving RF input signals 591-594, wherein 1010 is a tank circuit load that can comprise an inductor 1112 in parallel with a capacitance 1110 as shown in Fig. 11. The full-bridge amplifier 1008 and tank circuit 1010 can correspond to the basic bridge circuits and loads shown in Figs. 1, 3-5, and 7-9. In this case, the tank circuit 1110,1112 of Fig. 11 will be used as load 110 shown in Fig. 3, which has four NMOS transistors Q31-Q34. One of ordinary skill in the art would be able to relate those four transistors to switches S11-S14 shown in Fig. 1, and the associated alternating input signal shown in Fig. 2.

Therefore, Lincoln shows and discloses a method for buffering an input signal. The gates of each of Q31-Q34 (of Fig. 3) will each receive its respective input signal. As understood from Fig. 2, when the signal is at a first polarity (i.e. above 0), transistors Q31 and Q34 will be on, and transistors Q32 and Q33 will be off. At the second polarity (i.e. below 0), the states of the transistors will be reversed. Therefore, it is understood that: 1) Q34 generates a first current proportional to the input signal having the first polarity, and (approximately) zero current when the input signal has the second polarity; 2) Q32 generates a second current proportional to the input signal having the second polarity, and (approximately) zero current when the input signal has the first polarity; 3) Q31 generates a third current proportional to the first current; and 4) Q33 generates a fourth current proportional to the second current. Since tank circuit 1110,1112 of Fig. 11 is to be used as load 110, inductor 1112 and capacitance 1110 are coupled in parallel between the first/second terminals 108/106 of the inductor. It will also be noted that first current (from Q34) and fourth current (from Q33) are applied to first terminal 108, and the second current (from Q32) and third current (from Q31) are applied to second terminal 106. Lincoln discloses the relationship between the resonant frequency of the tank circuit and the frequency of the input signal (e.g. see column 1, lines 45-50; and column 10, lines 1-12). Therefore, it is understood by one of ordinary skill in the art that the (first) frequency of the input signal (e.g. 591-594) is the same as the tank circuit's resonant (second) frequency. Each transistor will transition from off to on to allow current to flow, when the transistor's respective input signal reaches and passes above the threshold voltage. During that temporary period (e.g. as the transistor begins to turn on to allow current flow), the transistor has a gate-source voltage that is approximately equal to its threshold voltage. This anticipates claims 3 and 4. Since it is

understood from Fig. 10, and related descriptions of the circuits, that input signals 591-594 are RF signals, it is also understood 1008,1010 of Fig. 10 provides a means for buffering an RF signal. Therefore, using the same type of reasoning as applied to claims 3 and 4 above, one of ordinary skill in the art would also know that the first current (from Q33) will generate the third current (through Q32), and the second current (from Q31) will generate the fourth current (through Q34). For example, with transistors Q31 and Q34 off, Q32 can only generate the third current when it receives the first current from Q33 (through load 110). As previously described, tank circuit 1110,1112 has an inductor and capacitance, and is operated at a resonating (second) frequency equal to the input signal's (first) frequency, thus anticipating claims 23-24.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 3-5, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denker et al. (Denker), another reference cited in the previous Office Action. Fig. 2 of Denker shows what can be considered a circuit that provides a method for buffering an input signal (from block 28). The gates of transistors 24-27 receive the input signal Ø1- Ø4 alternating between first and second polarities (e.g. see Fig. 5, wherein the first polarity can be considered the period when Ø1 is high, and the second polarity can be considered the period when Ø1 is low). [Note: Although Fig. 5 shows signals Ø1 and Ø3 as being non-overlapping signals with respect to signals Ø2 and Ø4, the column 5, lines 26-37 description

indicates/implies that when transistors 25 and 26 conduct, transistors 24 and 27 will be off, and vice versa. Also, neither set of series coupled transistors (24,25 and 26,27) will have their transistors conducting at the same time. This type of operation is well known and understood with respect to full-bridge type circuits as it prevents shoot through current from flowing from the positive power supply (e.g. VDD) to ground if either set of series connected transistors allows both transistors to conduct at the same time.] Therefore, it is understood that transistor 24 generates a first current proportional (e.g. high input: high current) to the first polarity of signal Ø1, and approximately zero when signal Ø1 is at the second polarity (e.g. low input: no current); transistor 26 generates a second current proportional (e.g. high input: high current) to the input signal when signal Ø4 is high during at least a portion of the period when signal Ø1 is at the second polarity, and approximately zero (e.g. low input: no current) when signal Ø4 is low during at least a portion of the period when signal Ø4 is a the first polarity portion of the period; transistor 27 generates a third current proportional to the first current (because transistors 27 and 24 will conduct at approximately the same time); transistor 25 generates a fourth current proportional to the second current (because transistors 25 and 26 will conduct at approximately the same time); the first and fourth currents (from 24 and 25) are applied to first terminal Q of inductor 23; and the second and third current s (from 26 and 27) are applied to second terminal /Q of inductor 24. As shown in Fig. 2, a capacitance (in 21 and 22) is coupled to/between the terminals of inductor 23. One of ordinary skill in the art would understand that the abstract's "The generator is operated at a frequency approximately equal the resonant frequency of the inductor combined with the capacitance of the load" relates to the frequency of input signal Ø1-Ø4 from generator 28, and the resonant frequency of inductor 23 and associated capacitance

(shown in 21 and 22). Also, column 6, lines 35-37 disclose the relationship between the input signal's frequency and the resonant frequency. Deeming the input and resonant frequencies as the first and second frequencies, respectively, they will be (approximately) equal to each other. However, the reference does not identify inductor 23 and its associated capacitance (in 21,22) as a tank circuit, nor does it clearly indicate the signals are RF. It would have been obvious to one of ordinary skill in the art to deem the inductor and capacitance as one type of an LC tank circuit (e.g. see 204 of Gabara et al.'s Figs. 5 and 6, also identified in the previous Office Action). Since the changing input signal must transition pass the respective transistor's threshold voltage in order to transition from an off state to an on state, the transistor will at least be temporarily biased with a gate-source voltage that is approximately equal to the threshold voltage, thus rendering claim 3 obvious. Since the first and second currents are generated by NMOS devices 24 and 26, claim 4 is rendered obvious. Similarly, PMOS devices 27 and 25 generate the third and fourth currents, rendering claim 5 obvious. Other than identifying the signal as an RF signal, the limitations of claims 23 and 24 correspond to those cited in claim 3 (e.g. it is understood the first current (from transistor 24) is used to generate the third current (from 27)). Therefore, all of those details do not need to be repeated here. If a high frequency operation, such as with radio frequencies (RF), was desired, it would have been obvious to one of ordinary skill in the art to clock the circuitry of Denker at the desired radio frequency. Therefore, clock generator 28 would provide RF signal Ø1- Ø4 to transistors 24-27, thus allowing the buffering of an RF signal, and rendering claims 23-24 obvious.

In so far as being understood, claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lincoln as applied to claim 4 above. As previously described, the reference of

Lincoln shows and discloses a buffering method with the first and second currents being generated by NMOS devices (i.e. Q34 and Q32). However, the reference shows the third and fourth currents also being generated by NMOS devices (i.e. Q31 and Q33). It would have been obvious to one of ordinary skill in the art to replace each of the series coupled transistors (i.e. Q31,Q32 and Q33,Q34) with a CMOS type inverter. In that case, Q31 and Q33 would be replaced by PMOS devices for generating respective third and fourth currents, thus rendering claim 5 obvious. The use of a CMOS type inverter will reduce the number of outputs 591-594 from RF signal generator 1006 (shown in Fig. 10) since each CMOS type inverter will only require one input signal/line. For example, when PMOS transistors Q31 is on, corresponding NMOS transistor Q32 will be off, and vice versa, since they would share the same input signal.

In so far as being understood, claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabara et al., another reference cited in the previous Office Action. The circuit shown in Fig. 6 can be deemed a method for buffering an input signal (provided by block 202). 203c receives an input signal (i.e. a clock signal) that alternates between what can be deemed first and second polarities (e.g. high and low; and/or voltages above and below the switching threshold of transistor 203c), wherein 203d receives a complement of the input signal. When the input signal is at the first polarity (i.e. high), 203c generates a first current proportional (i.e. high) to the input signal, and the current through 203d will be (approximately) zero because transistor 203d will be off due to the complement of the input signal. Similarly, when the input signal is at the second polarity (i.e. low), the current through 203c will be (approximately) zero, while 203d will generate a second current (i.e. high) proportional to the second polarity because transistor 203d will be conducting. The currents generated by the transistors within 312 are the

third and fourth currents that are deemed proportional to the first and second currents, respectively. [Even if the third and fourth currents through the transistors (within block 312) remain constant, they are still proportional to the first and second currents.] The first current (from 203c) and fourth current (from the left transistor of 312) are applied to a first (i.e. left) terminal of inductor 304, and the second current (from 203d) and third current (from the right transistors of 312) are applied to a second (i.e. right) terminal of inductor 304. Since capacitance 302 is coupled across (or between) the terminals of inductor 304, they will form a tank circuit 204 (e.g. see column 6, lines 39-40). However, the reference does not clearly show or disclose the tank circuit has a resonant (second) frequency that is approximately equal to the (first) frequency of the input signal. Applying the same type of reasoning as described in previous rejections above, current would be generated when a transistor is at least temporarily biased with its gate-source voltage being approximately equal to its threshold voltage. Since it would have been obvious to one of ordinary skill in the art to use the same frequencies for the input signal and resonant frequency of Gabara's circuit, claim 3 is rendered obvious. With the same frequencies, the circuit would operate at its most efficient speed since the switching speed of transistors 203c and 203d would correspond to the switching polarities across the tank circuit. These same frequencies would also provide the maximum power transfer of the switched current, and the resulting voltage across the tank circuit. The first and second currents are generated by NMOS devices (203c and 203d), rendering claim 4 obvious. The third and fourth currents are generated by PMOS devices (not labeled individually), rendering obvious claim 5. The input signals applied to the control terminals of 203c and 203d are injection signals. These injection signals can be either AC or data signals (e.g. see column 4, lines 5-6), understood to be

representative of respective sinusoidal and pulse type signals. An AC signal has first and second polarities. For example, the first polarity can be considered all levels of the AC signal above the switching threshold of a MOS transistor, and the second polarity can be considered all levels of the AC signal below the switching threshold. Therefore, it would be obvious to one of ordinary skill in the art to use an AC input signal as the injection signal applied to 203c (and 203d) of Gabara's circuit. Once the input signal's level reaches the switching threshold of 203c, that transistor will begin to turn on until the AC signal reaches its maximum (positive peak) level, and the transistor will then begin to turn off until the AC signal again reaches the switching threshold. [At the maximum (positive peak) level, the current flowing through 203c will be maximum.] One of ordinary skill in the art would understand the first current would thus be geometrically proportional to the first polarity (e.g. the first current will follow the AC signal when it's above the switching threshold). Once the input signal goes below the switching threshold, transistor 203c will turn off, thus providing (approximately) zero current when the input signal is at the second polarity. Using the same type of reasoning, transistor 203d will generate a second current geometrically proportional to the input signal at the second polarity, and (approximately) zero current when the input signal is at the first polarity (keeping in mind that 203d receives a complement of the actual input signal). Therefore, claim 6 is rendered obvious. The use of an AC input signal would provide a smoother transition between the current flows and output voltage. [Note: Although Gabara discloses a relationship between the invention and RF frequencies (e.g. 10 MHz (column 4, lines 35-40) and 3.25 Gb/s (column 9, lines 29-35)), the first and second currents do not generate the third and fourth currents, respectively as

recited within claims 23 and 25. The third and fourth currents are continuously provided by the transistors within block 312.]

In so far as being understood, claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denker, and in view of Clapp, III et al. (Clapp). Fig. 3 of Denker shows a circuit for buffering signals Ø1, Ø4, wherein the circuit comprises a first device 24 coupled between first output node Q and first supply node (e.g. ground), and having a control electrode coupled to a first input node (to receive Ø1); a second device 26 coupled between a second output node /Q and the first supply node, and having a control electrode coupled to a second input node (to receive Ø4); third device 25 coupled between second supply node VDD and first output node Q, and having a control electrode coupled to second output node /Q; fourth device 27 coupled between second supply node VDD and second output node /Q, and having a control electrode coupled to first output node Q; and an inductor 23 coupled between the first and second output nodes Q and /Q, respectively. First device 24 will conduct when signal Ø1 is above the switching threshold of transistors 24, and will turn off when the signal is below the switching threshold. When the signal transitions, the transistor will be at least temporarily biased with a gate-source voltage approximately equal to the transistor's threshold voltage. Similarly, second device 26 will conduct when complementary signal Ø4 is above the switching threshold of transistor 26, and will turn off when the signal is below the switching threshold. It also would have been obvious to one of ordinary skill in the art to use RF signals as signals Ø1 and Ø4 of Denker's circuit if RF output signals were desired for a particular application of the circuit. However, the reference does not show or disclose the fifth and sixth devices as recited within claim 27. Clapp shows a circuit in Fig. 3 with first-fourth devices 40, 42, 38, and 36 that

correspond to Denker's first-fourth devices 24, 26, 25, 27. Clapp also shows and discloses a clamping circuit 20 with fifth and sixth devices 50 and 52 coupled between the respective first/second output nodes and first/second devices. Those devices are used to clamp the output node voltages from dropping below the gate to source destruction voltage of transistors 38 and 36 (the third and fourth devices). For example, see column 4, lines 8-11 and 54-59. Therefore, it would have been obvious to one of ordinary skill in the art to add fifth and sixth devices to Denker's circuit. The fifth device would be coupled between first device 24 and first output node Q, and the sixth device would be coupled between second device 26 and second output node /Q, thus rendering claim 27 obvious. Since the first/second devices are NMOS, and the third/fourth devices 25/26 are PMOS, claim 28 is also rendered obvious. The use of fifth and sixth devices within Denker's could provide at least two proposes: 1) If the overall circuit of Denker is to be used with a power supply voltage VDD that could cause damage to the circuit's devices, the fifth/sixth devices will provide them with one means of protection from high voltage related damage; and 2) the fifth/sixth devices could be used as one means to shift the lowest output voltage farther above ground (due to the voltage drop of the device) if that was required by a circuit coupled to the outputs of Denker's circuit. Denker relates the circuit to liquid crystal displays, microprocessors, digital signal processors (DSPs), and integrated circuit chips (e.g. see column 1, lines 16-40). Since Denker refers to "integrated circuit chip" (see column 1, line 22) and "chip" (see column 1, line 50), it would be obvious to one of ordinary skill in the art that an integrated circuit would comprise the circuit of claim 28, thus rendering claim 29 obvious. It is understood that a large system (e.g. a processor – see column 1, line 18 of Denker) could use the

modified circuit of Denker. That large system can be deemed a transceiver as it will receive and supply (e.g. transmit) signals from related circuitry, rendering claim 30 obvious.

Allowable Subject Matter

Claims 17-21, 25, 31, 33-35, and 37-38 are allowable. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the buffering circuit also comprises the seventh device as recited within claim 17 (upon which claims 18-21, and 31 depend); 2) an RF buffering method generates the first-fourth currents, wherein the first and second currents are geometrically proportional to the RF signal, and has those currents applied to an inductor's terminals as recited within claim 25 (upon which claims 33-35 depend); or 3) the fifth device and current source as recited within claim 37 (upon which claim 38 depends).

Also, claims 32, 36, 39 and 40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Claim 32 depends on allowed claim 31; claim 36 depends on allowed claim 33; and both claims 39 and 40 depend upon allowed claim 37.

. Claims 1-2, 7-16, 22, and 26 have been cancelled.

Response to Arguments

The applicant's arguments filed Jun 3, 2003 have been fully considered but they are not persuasive. The applicant amended the claims to include a limitation citing "transistors that are biased to have gate-source voltages approximately equal to their threshold voltages", and then indicates that none of the examiner's prior art shows or provides this feature. The examiner disagrees.

The applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. In order for a transistor to transition from on to off, and vice versa, it must be biased in some manner that will ensure the transistor will turn on (or off). This is typically done by an input signal. In the case of an NMOS transistor, it will transition from off (i.e. minimal current flow) to on (i.e. desired current flow) when the input signal applied to its gate passes above the transistor's threshold voltage. At least during that temporary period of time, the transistor will be biased with a gate-source voltage that is approximately equal to the threshold voltage. [Note, at some point during this period of transitioning, the gate-source voltage will actually be equal to the threshold voltage since it must transition past it.] Therefore, one of ordinary skill in the art would understand that each of the references cited by the examiner shows/discloses transistors which will meet this recited limitation since they must transition past the threshold voltage when they transition from their off state to their on state.

The rejections described in this present Office Action are deemed proper.

The applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund

25 August2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800